REMARKS

Claims 2-8 are pending in this application. Applicant thanks the Examiner for indicating the presence of allowable subject matter in claims 2-6.

Claims 2-8 were rejected under 35 USC 112, second paragraph, as being indefinite. Applicant respectfully traverses this rejection.

Claim 8 recites a circuit layout configuration for matching two transistors including a first transistor comprising eight first sub-transistors and a second transistor comprising eight second sub-transistors. The eight first sub-transistors and the eight second sub-transistors are arranged in a four by four matrix, the eight second sub-transistors occupy eight diagonal positions of the four by four matrix, and the eight first sub-transistors occupy positions of the four by four matrix that are not the diagonal positions.

Applicant submits that the claim language, read in conjunction with the text on pages 6-7 of the specification and by referring to applicant's Fig. 1, is not indefinite. Fig. 1 shows a multiple-common-centroid layout configuration. M1 and M2 are MOS field effect transistors that are to be matched. The first transistor M1, that is a main-transistor, is divided into eight sub-transistors MS11, MS12, MS13, MS14, MS15, MS16, MS17 and MS18. Gates, drains and sources of these sub-transistors are connected in common to form the first transistor M1. Similarly, the second transistor M2, that is a main-transistor, is also divided into eight sub-transistors MS21, MS22, MS23, MS24, MS25, MS26, MS27 and MS28. Gates, drains and sources of these sub-transistors are connected in common to form the second transistor M2. The first transistor M1 and the second transistor M2 can form differential input pair transistors of a differential amplifier. When a current mirror is formed with the first transistor M1 and the second transistor M2, the gates of the sub-transistors are connected in common with each other.

The abovementioned 16 sub-transistors forming the first and second transistors M1 and M2 are arrayed in a matrix with four rows and four columns, when viewed as a whole. The matrix is formed of four cells. A first cell C1 is composed of the sub-transistors MS11 and

MS12 and the sub-transistors MS21 and MS22. A second cell C2 is composed of the sub-transistors MS13 and MS14 and the sub-transistors MS23 and MS24. A third cell C3 is composed of the sub-transistors MS15 and MS16 and the sub-transistors MS25 and MS26. A fourth cell C4 is composed of the sub-transistors MS17 and MS18 and the sub-transistors MS27 and MS28.

To explain the first cell C1 in detail, the sub-transistor MS21 disposed at a first row and a first column, the sub-transistor MS22 disposed at a second row and a second column, the sub-transistor MS11 disposed at the first row and the second column and the sub-transistor MS12 disposed at the second row and the first column have a common center P1.

The sources and drains of these sub-transistors are arrayed parallel to a column direction while their gates are arrayed parallel to a row direction. The second cell C2, the third cell C3 and the fourth cell C4 are formed with symmetrical configuration based on the first cell C1. Each of the second cell C2, the third cell C3 and the fourth cell C4 has common centers P2, P3 and P4, respectively.

Accordingly, the claim language, as supported by applicant's written description, calls for the rejection of claim 8 for indefiniteness to be withdrawn. This logic also disposes of the rejection of claims 2-7, which depend directly or indirectly from claim 8.

Claims 2-8 were rejected under 35 USC 102(b) as anticipated by Ho U.S. Patent No. 5,644,517. However, as explained in paragraph 6 of the Action, and as further explained in paragraphs 7-8, only claims 7 and 8 stand rejected by Ho. Applicant respectfully traverses this rejection.

Applicant's claims relate to a circuit layout configuration to improve matching characteristics of a transistor pair in a circuit having the transistor pair, such as a current mirror circuit and a differential amplifier. As applicant describes, the multiple-common-centroid layout of this invention has the effect that performance comparable to the four-segment layout can be obtained while the layout area can be made small. In particular, a low offset operational

amplifier can be realized by applying the layout of this invention to a differential transistor pair and a transistor pair forming a current mirror of the operational amplifier. This is an analog circuit that that uses continuous value voltages and currents as opposed to a digital device where devices tend to have discrete, on/off values.

In contrast, Ho discloses a matrix transpose system and method for use on a 2-dimensional NxN mesh multiprocessor parallel network with circuit-switched-like routing in the recursive and iterative forms. Ho provides a method for matrix transpose on mesh multi-node parallel computer networks that provides a two-level decomposition technique of a matrix wherein the transposition of all off-diagonal submatrices can be performed concurrently, and wherein the transposition of all successive on-diagonal submatrices can be performed iteratively or recursively. Ho provides a matrix transpose method that is commercially feasible to implement on mesh-connected multi-processor architectures for large scale numerical computation applications involving the matrix transpose operation.

As apparent from above, both the structure and function of applicant's device is very different from Ho's device. For example, applicant's transistor pair, such as a current mirror circuit and a differential amplifier, is not the same as Ho's mesh configuration, in which each node is a processor involved in a matrix transpose operation.

In Ho, there is no disclosure or suggestion of a circuit layout configuration for matching two transistors. There is no disclosure or suggestion of a first transistor comprising eight first sub-transistors and a second transistor comprising eight second sub-transistors. There is similarly no disclosure or suggestion where the eight first sub-transistors and the eight second sub-transistors are arranged in a four by four matrix and the eight second sub-transistors occupy eight diagonal positions of the four by four matrix, and the eight first sub-transistors occupy positions of the four by four matrix that are not the diagonal positions.

The Action alleges "Re claim 8, as shown in Fig. 2B, Ho discloses a circuit layout for matching two transistors . . ." This falls far short of the specificity necessary to support a 35

USC 102 rejection. Indeed, nowhere in the Action does the Examiner point to any disclosure in Ho of matching two transistors, as required to support a proper rejection under 35 USC 102.

Accordingly, Ho cannot anticipate claim 8, and the rejection should be withdrawn. This logic also disposes of the rejection of claims 2-7, which depend directly or indirectly from claim 8.

In view of the above, each of the claims in this application is in condition for allowance. Accordingly, applicant solicits early action in the form of a Notice of Allowance.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing Docket No. **606402028400**.

Respectfully submitted,

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